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TECHNOLOGY CENTER 2800

Inventor application of: Sailesh Chittipeddi

Serial No.: 09/596,382

Filed: June 16, 2000

For: A PROCESS FOR MANUFACTURING AN INTEGRATED
CIRCUIT INCLUDING A DUAL-DAMASCENE STRUCTURE
AND A CAPACITOR

Group No.: 2812

Examiner: Tsai, H. Jey

Commissioner for Patents
Washington, DC 20231

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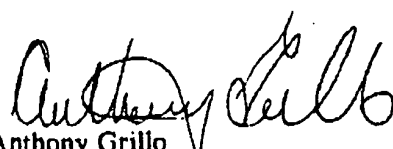
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of Hitt Gaines & Boisbrun, P.C.; P.O. Box 832570, Richardson, Texas 75083 as our associate attorneys in the above-mentioned application, with full power to prosecute said application, to make alterations and amendments therein, and to transact all business in the Patent and Trademark Office connected therewith.

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